Interfacing the LTC1290 to the Z-80 MPU

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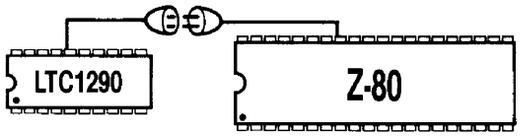

Introduction

This application note describes an interface between the LTC1290 12-bit data acquisition system and the Z-80 microcomputer. The interface is capable of completing a 12-bit conversion and shifting the data to Z-80 in 260μs. Configuration of the LTC1290 and the Z-80 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given, including data throughput rates.

Interface Details

The LTC1290 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred serially in a synchronous, full duplex format over D_{IN} and D_{OUT}.

The Z-80 does not have a serial port. Therefore it is necessary for the user to construct a serial port with TTL gates as shown in the schematic of Figure 1.

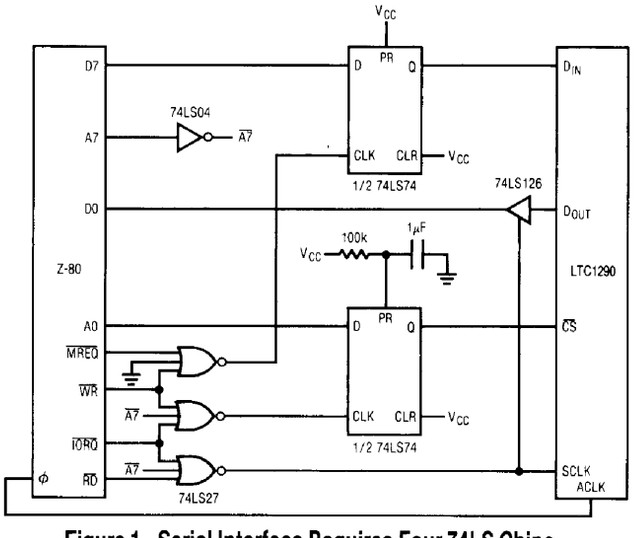

Figure 1. Serial Interface Requires Four 74LS Chips

Hardware Description

$\overline{CS}$ is set or cleared by placing a 1 or a 0 on address line A0 and writing to an I/O port that has an even address of 128 or higher. The LTC1290 SCLK is generated by reading from an I/O port that has an address greater than 128. Data is clocked into the LTC1290 one bit at a time by placing the desired bit on D7 of the Z-80 and writing to any memory location. The serial data output of the LTC1290 is fed into D0 of the Z-80 through the 74LS126. The 74LS126 prevents the LTC1290 from writing to the data bus of the Z-80 except when the microprocessor requires data from the A/D. The ACLK of the LTC1290 is also the clock for the Z-80.

The code for this interface was developed on a Multitech MPF-1 single board development system.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer. The Z-80 clock rate was 1.79MHz. Using a Z-80B and running it at a 6MHz clock rate, it is possible to reduce this time to approximately 100μs. This would require generating ACLK externally or dividing down the ϕ signal.

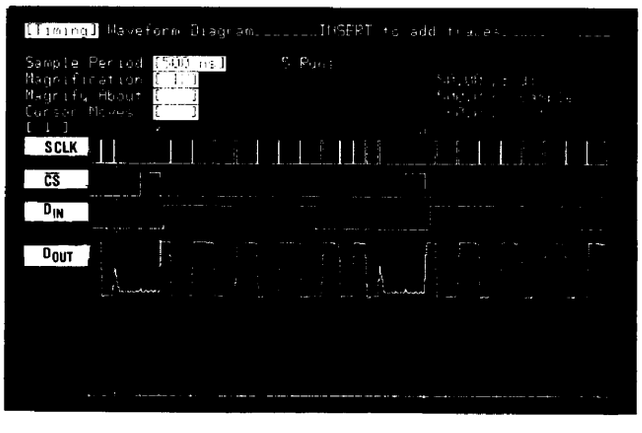

Figure 2. Throughput Time is Limited by the Z-80 MPU. A 12-Bit Conversion Result is Transmitted Every 260μs.

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1290 please see the data sheet.

Software Description

The software serially shifts the D_{IN} configuration word to the LTC1290 while simultaneously reading the previous data back. Additionally, the software waits while the LTC1290 performs its next conversion before attempting the next data exchange cycle.

The Z-80 code is shown in Figure 5. First the C register is cleared. The D register is loaded with the D_{IN} word (FEH) for the LTC1290. This word as shown in Figure 3 configures the input MUX of the LTC1290 to accept a signal on CH7 with respect to COM, perform a unipolar conversion and shift the data out MSB-first as a 12-bit word. Next $\overline{CS}$ is brought low by writing to I/O port 128 (80H). The MSB of the D register containing the D_{IN} word is the output on bit 7 of the data bus of the Z-80. The first bit of the LTC1290 D_{OUT} word is then read into the A register. The act of reading this bit also generates an SCLK pulse. The D_{OUT} bit is then shifted into the carry bit and from there it is rotated into the LSB of the B register. This process is repeated seven more times until the D_{IN} bits have been shifted out and the 8 MSBs of the D_{OUT} word have been shifted into the B register. The last four bits of the D_{OUT} word are then shifted through the carry bit into the LSB position of the C register. Then it is rotated right through the carry bit into the four MSB positions of the C register. $\overline{CS}$ is then brought high. The 12-bit D_{OUT} word is now stored left justified in the Z-80 as shown in Figure 4.

1	1	1	1	1	1	1	0
S/D	O/S	S1	S2	UNI	MSBF	WL1	WL0

Figure 3. D_{IN} Word for LTC1290 Stored in D Register of Z-80

MSB

11	10	9	8	7	6	5	4	REG B

LSB

3	2	1	0	FILLED WITH ZEROS	REG C

D_{OUT} from LTC1290 stored in Z-80 registers

Figure 4. Memory Map of Z-80

After the last SCLK pulse is ended, 52 ACLK cycles must be allowed for the LTC1290 to perform the desired A/D conversion. During this time $\overline{CS}$ is taken high. The software must ensure that this occurs.

Power Shutdown

The LTC1290 can be shutdown by inputting the appropriate D_{IN} word (FDH). A dummy conversion prior to a request for power shutdown is required because the data from the previous conversion will be shifted out as a 10-bit word during the power shutdown request. Upon power up, the LTC1290 is ready for conversion and the D_{OUT} word will be valid on the second request for conversion.

Summary

An interface between the LTC1290 12-bit data acquisition system and the Z-80 microprocessor with a combined data conversion and transfer time of 260μs was demonstrated. The interface used four 74LS chips to interface the two devices. The 12 data bits of the LTC1290 are shifted MSB-first one bit at a time. The data is stored left justified in the Z-80's internal registers.

Reference

Hoover, Guy, "Interfacing the LTC1090 to the Z-80," Application Note 260, Linear Technology Corp.

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LABEL    MNEMONIC          COMMENTS
BEGIN    LD     C,00H      INITIALIZE REG C
         LD     D,FE       LOAD DIN IN REG D
         OUT    (80H),A    CS GOES LOW

BLOCK1   LD     (HL),D     OUTPUT DIN BIT
         IN     A,(80H)    READ DOUT BIT AND OUTPUT ONE SCLK
         RRA               SHIFT DATA TO CARRY
         RL     B          SHIFT DATA TO REG B
         RLC    D          SHIFT DIN WORD LEFT
         .
         .
         .
         REPEAT CODE LABELLED BLOCK1 SEVEN TIMES FOR A
         TOTAL OF EIGHT
         .
         .
         .

BLOCK2   IN     A, (80H)   READ DOUT BIT AND OUTPUT ONE SCLK
         RRA               SHIFT DATA TO CARRY
         RL     C          SHIFT DATA TO REG C
         .
         .
         REPEAT CODE LABELLED BLOCK2 THREE TIMES FOR A
         TOTAL OF FOUR
         .
         .
         RR     C          SHIFT REG C DATA RIGHT
         RR     C          SHIFT REG C DATA RIGHT
         RR     C          SHIFT REG C DATA RIGHT
         RR     C          SHIFT REG C DATA RIGHT
         OUT    (81H)      CS GOES HIGH
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Figure 5. Z-80 Code